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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/534,983	05/14/2005	Seong-Yong Hwang	8054-109	1861

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EXAMINER	
TYNAN, MATTHEW	
ART UNIT	PAPER NUMBER
2871	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/534,983	HWANG ET AL.	
	Examiner	Art Unit	
	Matthew Tynan	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 May 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/14/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 5/14/2005 was filed after the mailing date of the instant application on 5/14/2005. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

3. The drawings are objected to because in drawing 11A and 12A, the reference numerals 800, 810, 820 and 900, 910, and 920 do not correctly correspond to the text of the specification. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet"

pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claim 5 is objected to because of the following informalities: lines 8-9 recite a "conductive bump electrically connected to a driving IC that applies a predetermined signal to the electrode pad by using a non-conductive resin." This phrasing seems to imply the IC applies the signal "by using a non-conductive resin". The examiner objects to this phrasing and suggests for purposes of clarity that it be rephrased so that it is not suggested that the non-conductive resin supplies electricity or a signal.

5. Claim 13 is objected to because of the following informalities: line 4 reads, "the LCD apparatus comprising" which should be corrected to read, "the method comprising."

6. Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 2, 4, and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Nishiki et al. (U.S. Patent No. 5,798,812).

9. Regarding claim 1, Nishiki et al. discloses:

- A thin film transistor substrate (Fig. 1) comprising: a plurality of electrode pads (8, 9) disposed on end portions of gate (1) and data lines (2) arranged on a substrate; and a conductive bump including a protrusion member (10, Fig. 2D) disposed on the electrode pad with a predetermined thickness and a conductive coating layer (6a, Fig. 2D) disposed on the protrusion member to be electrically connected to the electrode pad (8, 9), the conductive bump being electrically connected to a driving integrated circuit (IC) (col. 6, lines 66-67) that applies a predetermined signal to the electrode pad by using a non-conductive resin (insulative resin 22, Fig. 3).

10. Regarding claim 2, Nishiki et al. discloses the protrusion member (10) is disposed on the electrode pad (8, 9) such that a peripheral portion of the electrode pad is exposed. See Fig. 2D.

11. Regarding claim 4, Nishiki et al. discloses the protrusion member comprises a plurality of projections (i.e. there are a plurality of protrusion members 10) spaced apart by a predetermined distance, a portion of the electrode pad being exposed through a space between the projections. See Fig. 2D.

12. Regarding claim 5, Nishiki et al. discloses a method of manufacturing a thin film transistor substrate, the method comprising:

- Forming a gate line (1), a data line (2) and a plurality of electrode pads (8,9) disposed on end portions of the gate and data lines; and forming a conductive bump including a protrusion member (10) disposed on the electrode pads to have a predetermined thickness and a conductive coating layer (6a) disposed on the protrusion member to be electrically connected to the electrode pad, the

conductive bump electrically connected to a driving IC (col. 6, lines 66-67) that applies a predetermined signal to the electrode pad by using a non-conductive resin (see Fig. 2A).

13. Regarding claim 6, Nishiki et al. teaches:

- The conductive bump is formed by: forming a photoresist organic layer (10; see col. 6, lines 53-56) on the electrode pad (9); patterning the photoresist organic layer to form a protrusion member on the electrode pad (see Fig. 2A); forming a conductive layer covering the protrusion member (see Fig. 2B); and patterning the conductive layer to form a conductive coating layer on the protrusion member, the conductive coating layer being electrically connected to the electrode pads.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Woo et al. (U.S. Pub. No. 2002/0122143) in view of Chang (EP 0827190 A2) and Hatada et al. (U.S. Patent No. 5,089,750).

16. Regarding claim 1, Woo et al. teaches a thin film transistor substrate (21, Fig. 5) comprising:

- A plurality of electrode pads (GP1, GP2, DP1, DP2, etc. Fig. 3) disposed on end portions of gate lines (G1, G2, etc.) and data lines (D1, D2, etc.) to be electrically connected to a driving integrated circuit (**[0049]**, lines 1-2).

17. Woo et al. does not disclose:

- A conductive bump including a protrusion member disposed on the electrode pad with a predetermined thickness and a conductive coating layer disposed on the protrusion member to be electrically connected to the electrode pad, the conductive bump being electrically connected to a driving integrated circuit (IC) that applies a predetermined signal to the electrode pad by using a non-conductive resin.

18. However, Chang discloses a conductive bump (Fig. 1A) including a protrusion member (32) disposed on the electrode pad (26) with a predetermined thickness and a conductive coating layer (36) disposed on the protrusion member, the conductive bump being electrically connected to the electrode pad, the conductive bump being electrically connected to a driving IC (col. 2, lines 37-39). This configuration allows a bond to be made with low bonding force, greately reduces the force tending to separate the connections after bonding, and results in extremely reliable physical and electrical connections between the integrated circuit element and the substrate (col. 2, lines 29-34).

19. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device taught by Woo et al. using the conductive bump taught by Chang in order to create, for instance, extremely reliable physical and electrical connections between the integrated circuit element and the substrate.

20. Chang suggests bonding can be done using a non-conductive adhesive between the IC and the substrate (abstract, lines 13-16).

21. Hatada et al. suggests that the use of an insulating resin for providing the connection between the IC and the substrate prevents leakage between adjacent leads and adjacent electrodes so that the pitch of the electrodes may be reduced (col. 2, lines 8-12).

22. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device taught by Woo et al. and Chang using the non-conductive resin taught by Hatada et al. in order to prevent leakage between adjacent electrodes.

23. Regarding claim 2, Chang teaches the protrusion member (32, Fig. 1A) is disposed on the electrode pad (26) such that a peripheral portion of the electrode pad is exposed.

24. Regarding claim 3, Chang teaches that the protrusion member comprises and embossing pattern on an upper surface thereof (Fig. 3).

25. Regarding claim 4, Chang teaches that the protrusion member (32) comprises a plurality of projections (Fig. 4) spaced apart by a predetermined distance, a portion of the electrode pad being exposed through a space between the projections.

26. Regarding claim 5, Woo et al. teaches forming a gate line (G1), a data line (D1), and a plurality of electrode pads (GP1, DP1) disposed on the end portions of the gate and data lines.

27. Woo does not teach forming a conductive bump including a protrusion member disposed on the electrode pad with a predetermined thickness and a conductive coating layer disposed on the protrusion member to be electrically connected to the electrode pad, the conductive bump being electrically connected to a driving integrated circuit (IC) that applies a predetermined signal to the electrode pad by using a non-conductive resin.

28. However, Chang discloses a conductive bump (Fig. 1A) including a protrusion member (32) disposed on the electrode pad (26) with a predetermined thickness and a conductive coating layer (36) disposed on the protrusion member, the conductive bump being electrically connected to the electrode pad, the conductive bump being electrically connected to a driving IC (col. 2, lines 37-39). This configuration allows a bond to be made with low bonding force, greately reduces the force tending to separate the connections after bonding, and results in extremely reliable physical and electrical connections between the integrated circuit element and the substrate (col. 2, lines 29-34).

29. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device taught by Woo et al. using the conductive bump taught by Chang in order to create, for instance, extremely reliable physical and electrical connections between the integrated circuit element and the substrate.

30. Chang suggests bonding can be done using a non-conductive adhesive between the IC and the substrate (abstract, lines 13-16).

31. Hatada et al. suggests that the use of an insulating resin for providing the connection between the IC and the substrate prevents leakage between adjacent leads and adjacent electrodes so that the pitch of the electrodes may be reduced (col. 2, lines 8-12).

32. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device taught by Woo et al. and Chang using the non-conductive resin taught by Hatada et al. in order to prevent leakage between adjacent electrodes.

33. Regarding claim 6, Chang teaches forming the conductive bump by:

- Forming a photoresist organic layer (32) on the electrode pad (26; see Fig. 9B).

- Patterning the photoresist organic layer to form a protrusion member (Fig. 9C).
- Forming a conductive layer covering the protrusion member (Fig. 9D).
- Patterning the conductive layer to form a conductive coating layer on the protrusion member, the conductive coating layer being electrically connected to the electrode pads (Fig. 9E).

34. Claims 7-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Woo et al. (U.S. Pub. No. 2002/0122143) in view of Chang (EP 0827190 A2).

35. Regarding claim 7, Woo et al. discloses an LCD apparatus including a pixel region (A, Fig. 6) having a plurality of thin film transistors (claim 12, lines 1-2), including a pad region (P, Fig. 6) having a plurality of electrode pads, the LCD apparatus comprising:

- An LCD panel (**[0048]**, line 1) including a TFT substrate (61, shown in Fig. 6 and 7), a color filter substrate (61a) and a liquid crystal layer (LC) interposed between the TFT substrate and the color filter substrate.
- A driving IC electrically connected to the electrode pad (**[0049]**, lines 1-2).
- An adhering member (ACF, **[0052]**, line 4) adhering the driving IC to the electrode pads (GP1, DP1, etc.).

36. Woo et al. does not teach a protrusion member, a conductive bump disposed on the protrusion member, the conductive bump having a conductive coating layer that is electrically connected to the electrode pad.

37. However, Chang teaches a protrusion member (32), a conductive bump disposed on the protrusion member (see Fig. 1A), the conductive bump having a conductive coating layer (36) that is electrically connected to the electrode pad (26).

38. This configuration allows a bond to be made with low bonding force, greately reduces the force tending to separate the connections after bonding, and results in extremely reliable physical and electrical connections between the integrated circuit element and the substrate (col. 2, lines 29-34).

39. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device taught by Woo et al. using the conductive bump taught by Chang in order to create, for instance, extremely reliable physical and electrical connections between the integrated circuit element and the substrate.

40. Regarding claim 8, Chang teaches the protrusion member comprises an elastic organic material (col. 2, lines 28-29) so that the conductive bump is compressed by a distance when the driving IC is pressed down and is restored corresponding to the distance when the driving IC is released, thereby maintaining an electrical connection between the conductive bump and the driving IC. Because the protrusion member comprises an elastic organic material, it inherently has the property that pressure will compress it, but upon release of that pressure, the protrusion will be restored.

41. Regarding claim 9, Chang teaches the protrusion member (32, Fig. 1A) is disposed on the electrode pad (26) such that a peripheral portion of the electrode pad is exposed.

42. Regarding claim 10, Chang teaches that the protrusion member comprises and embossing pattern on an upper surface thereof (Fig. 3).

43. Regarding claim 11, Chang teaches that the protrusion member (32) comprises a plurality of projections (Fig. 4) spaced apart by a predetermined distance, a portion of the electrode pad being exposed through a space between the projections.

44. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Woo et al. (U.S. Pub. No. 2002/0122143) in view of Chang (EP 0827190 A2).

45. Regarding claim 13, Woo et al. forming an LCD apparatus including a pixel region (A, Fig. 6) having a plurality of thin film transistors (claim 12, lines 1-2), including a pad region (P, Fig. 6) having a plurality of electrode pads, the method comprising:

- Forming a TFT substrate (61, shown in Fig. 6 and 7).
- Forming a color filter substrate (61a).
- Forming a liquid crystal layer (LC) interposed between the TFT substrate and the color filter substrate.
- A driving IC electrically connected to the electrode pad (**[0049]**, lines 1-2).

46. Woo et al. does not teach a protrusion member, a conductive bump disposed on the protrusion member, the conductive bump having a conductive coating layer that is electrically connected to the electrode pad.

47. However, Chang discloses a conductive bump (Fig. 1A) including a protrusion member (32) disposed on the electrode pad (26) with a predetermined thickness and a conductive coating layer (36) disposed on the protrusion member, the conductive bump being electrically connected to the electrode pad, the conductive bump being electrically connected to a driving IC (col. 2, lines 37-39). This configuration allows a bond to be made with low bonding force, greately reduces the force tending to separate the connections after bonding, and results in extremely reliable physical and electrical connections between the integrated circuit element and the substrate (col. 2, lines 29-34).

48. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device taught by Woo et al. using the conductive bump taught by Chang in order to create, for instance, extremely reliable physical and electrical connections between the integrated circuit element and the substrate.

49. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Woo et al. and Chang as applied to claim 13 above, and further in view of Park et al. (U.S. Patent No. 6,380,559).

50. Regarding claim 14, the combination of Woo et al. and Chang teaches:

- Forming an insulating film (Woo et al. 83, Fig. 7-8) on the entire surface of the substrate (61), including the pixel and pad regions.
- Patterning the insulation layer to form an insulating layer in the pixel region (Woo et al.) and patterning a photoresist organic layer to form a protrusion member (32, Chang) in the pad region (Chang).
- Forming a conductive layer (36, Chang; and **[0070]**, lines 1-5, Woo et al.) over the insulating layer and the protrusion member.
- Patterning the conductive layer (36, Chang; and **[0070]**, lines 1-5, Woo et al.) to form a pixel electrode (Woo et al., **[0061]**, lines 2-3) and a conductive coating layer on the protrusion member (Woo et al., **[0061]**, lines 1-5, and Chang 36).

51. The combination of Woo et al. and Chang is silent regarding the material used for the insulating film.

52. However, Park et al. teaches that an insulation film can be replaced by a photosensitive organic layer (80), which avoids processing of a separate photoresist layer to pattern the insulation layer, thus simplifying the manufacturing process (col. 17, lines 64-67).

53. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device taught by Woo et al. and Chang by using a photoresist organic layer to provide the insulation layer as taught by Park et al. in order to simplify the manufacturing process.

54. Regarding claim 15, Woo et al. teaches that the conductive layer (63) of the electrode pads should be ITO, because such a material has better adhesive properties than a metal (**[0052]**).

55. Regarding claim 16, Chang teaches the conductive layer (36) comprises a metal (col. 4, lines 1-5). Chang teaches that multiple layers of metal may be used, each to increase adhesiveness, to increase conductivity, and to act as a barrier layer (col. 4, lines 50-56). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a metal layer to increase adhesiveness, conductivity, or to act as a barrier.

56. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Woo et al., Chang, and Park et al. as applied to claim 14 above, and further in view of Komatsu (U.S. Patent No. 6,384,888).

57. Regarding claim 17, the combination of Woo et al., Chang, and Park et al. teaches the use of a single metal layer, as discussed above regarding claim 16. The combination does not teach a stack including a first layer of ITO or IZO and a second layer including metal.

58. However, Komatsu teaches that the material of the pad region includes three layers, including two of metal and one of ITO. The layer of ITO prevents the oxidation of the lower

metal layers, and thus reduces the contact resistance between the electrode pads and the driving circuits (col. 5, lines 7-16).

59. It would have been obvious to one of ordinary skill in the art at the time the invention was made to cover a metal layer taught by Chang such as in re claim 16 using the ITO layer taught by Komatsu to reduce contact resistance between the electrode pads and the driving circuits.

60. Claims 12 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Woo et al. and Chang as applied to claims 7 and 13 above, and further in view of Hatada et al. (U.S. Patent No. 5,809,750).

61. Regarding claim 12, the combination of Woo et al. and Chang does not teach that the adhering member comprises a non-conductive resin that is softened during a thermal compression and has gradually hardened.

62. However, Hatada et al. suggests that the use of an insulating resin for providing the connection between the IC and the substrate prevents leakage between adjacent leads and adjacent electrodes so that the pitch of the electrodes may be reduced (col. 2, lines 8-12). Hatada et al. further teaches that the non-conductive resin may be applied by pressing the electrodes one to another (col. 3, lines 28-32) and by applying heat (col. 3, 36-37).

63. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device taught by Woo et al. and Chang using the non-conductive resin taught by Hatada et al. in order to prevent leakage between adjacent electrodes.

Conclusion

64. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Park et al. (U.S. Pub. No. 2001/0046016) teaches much of the claimed subject matter and elements.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew Tynan whose telephone number is 571-270-1433. The examiner can normally be reached on Mon-Thurs. 7:30-5pm; 7:30-4pm on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, George Nguyen can be reached on 571-272-4491. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JAMES A. REAGAN
PRIMARY EXAMINER